High Voltage Dual-Gate Turn-off Thyristors

Oscar Apeldoorn, Peter Steimer
ABB-Industrie AG
CH-5300 Turgi

Peter Streit, Eric Carroll, Andre Weber
ABB-Semiconductors AG
CH-5600 Lenzburg

Abstract The quest of the last ten years for high power snubberless semiconductor switches has resulted in IGCTs (Integrated Gate-Commutated Thyristors) and IGBTs (Insulated-Gate Bipolar Transistors) currently available up to 6 kV. Both devices have inherently short switching times but are nevertheless frequency limited by their switching losses. 10 kV IGCTs have been shown to be useable up to about 5.5 kV DC and 400 Hz [1]. However market needs for PWM (pulse width modulation) at about 1 kHz cannot be satisfied above 3 kV DC, due to the inherent turn-off losses of the aforementioned bipolar components. The fundamental barrier presented by the charge stored in the n-base of IGBTs and IGCTs must be reduced at turn-off without increasing conduction losses. The use of a second, anode-side gate (n-gate) to reduce the high plasma density at turn-off has already been described for conventional snubbed GTOs [2,3] but the technique has not yet been applied to a snubberless device such as the IGCT. This paper will show the turn-off loss reductions which can be obtained by "grafting" a second gate to the conventional IGCT and will compare these results to those of a new type designed specifically for "gate-assisted turn-off".

I. INTRODUCTION
A. Performance Considerations

The motivation for such high voltage devices lies in applications for 6600 – 7200 V_RMS lines. Today such an equipment can be realized with two series-connected 4.5 – 5.5 kV IGCTs which easily achieve 1 kHz PWM but require R-C snubbers for the series connection [4]. Though simple enough, the number of components required at the switch level increases nearly three-fold and becomes an obstacle to the widespread use of power electronics at this voltage level.

Today’s 3-level IGCT inverters for the 3300 V line can operate at up to 900 Hz PWM [4] or higher. At 4160 V_RMS line, PWM frequencies of 500 Hz are typical [5]. To realize inverters on the 7200 V_RMS line would require two series connected 6 kV IGCTs. Currently such devices use about 33% of their thermal budget in conduction losses and 66% in switching losses at 500 Hz. 10 kV devices operating on the 6.9 – 7.2 kV_RMS line would exhibit a slightly higher dynamic loss ratio [1] of about 75% at the same frequency. If these dynamic losses could be reduced by a factor two, a 10 kV device could theoretically operate at 1 kHz on the 7.2 kV line with 80% of the power of a 4160 V design (using 6 kV IGCTs of the same size wafer).

B. Cost Considerations

Within high power products the costs of the semiconductors together with that of its drivers, control and mechanics have a high impact on the final bill of material (BoM). A step towards a 7.2 kV application by using 4.5 kV GCTs would roughly imply a doubling of all semiconductors, drivers, control and mechanics. Although the size of the semiconductors decreases and also the mechanics could be simplified at certain places, the calculated impact for real equipment can still be a BoM increase of 150% - 190%. Even the volume of the product increases drastically.

The use of HV dual-gate devices instead of series connection has only modest impact on the product mechanics, drivers and control. A redesign of standard 3.3 – 4.1 kV products into 6.6 – 7.2 kV products would entail some increase od semiconductors cost per switched MW but there would only be a few changes in mechanics, drivers and control and only a marginal variation in the total BoM and equipment size.

C. Motivation

Based on the above considerations, it is believed that the added complexity and cost of a dual-gate switch will be economically acceptable (compared to two series-connected IGCTs) if the losses per switched power of a 10 kV device are equal or less than those of 4.5 kV devices.

D. Structures

The structure of the Dual Gate-Turn-off Thyristor is shown in Fig. 1. This device can be processed in the same way as a conventional (single-gate) IGCT.

![Fig. 1. Semiconductor-structure of a “symmetrical” Dual Gate IGCT](image-url)
II. TESTS

A. Gate Units

Device testing is performed with a gate unit connected to gate G\textsubscript{1} and with an additional gate unit connected to gate G\textsubscript{2}. The timing of gate G\textsubscript{2} with respect to gate G\textsubscript{1} can be delayed from 0 to 6 µs.

B. Test Circuit

Fig. 2. shows the Device Under Test (DUT) in its test circuit. During commutation after GCT turn-on the inductance Lc1 controls the di/dt of the Free Wheel Diode (FWD). The capacitor Ccl clamps over-voltages at DUT turn-off.

C. Gate Timing

The DUT is turned-off by reverse-biasing the gate-cathode via the GU\textsubscript{1} (V\textsubscript{GK} negative). At turn-off GU\textsubscript{2} has an output voltage which is always positive (V\textsubscript{GA} = 0 to +20V). At a time Δt prior to G\textsubscript{1} turn-off, GU\textsubscript{2} is switched on. In this way, charge carriers in the anode side pn-junction are removed before switching off the complete device via GU\textsubscript{1}. GU\textsubscript{2} is kept in this state until at least 50 µs before the next turn-on pulse. The values of Δt and V\textsubscript{GA} effect the turn-off losses.

III. EXPERIMENTAL RESULTS

Devices of both asymmetric and symmetric design were tested.

A. Asymmetric Dual-Gate

Figs. 4 and 5 show the results on asymmetric dual gate IGCT devices. The identification "single" refers to DUT turn-off without G2 assist. Fig. 4 shows turn-off waveforms as a function of Δt for V\textsubscript{GA} = +15 V. Synchronous triggering of both gates (Δt = 0) already resulted in a significant reduction in tail-current and losses. Progressive increases in Δt further reduced tail losses but provoked a small premature rise of the anode voltage increasing the losses during the voltage rise.

No further loss reductions were obtained beyond Δt = 6 µs as seen in Fig. 4.

The measurements were repeated for a fixed value of Δt = 6 µs but with V\textsubscript{GA} varied from 0 to 15 V and the results are shown in Fig. 5. The greatest loss reduction is achieved with the highest voltage as this maximizes the speed at which the charge carriers are removed from the anode-side pn-junction.

The above tests carried out on a Dual-Gate IGCT processed from a standard GCT revealed switching loss reductions of up to 35% at 1500V/1650A/25°C by pre-triggering G\textsubscript{2} 6 µs ahead of G\textsubscript{1} as compared to G\textsubscript{1} operation alone.

B. Symmetric Dual-Gate

The tests were repeated with devices of symmetric design with both 4.5 and 5.5 kV ratings and compared with a standard 4.5 kV IGCT (type 5SHY 35L4510).

Fig. 6 shows the turn-off at 2 kV DC of a 4.5 kV symmetric dual-gate device with the two gates switched simultaneously (Δt = 0µs) for a G\textsubscript{2} voltage of 0V. In this experiment, the gate-unit merely shorts out the pnp transistor but does not actively extract n-base charge. The anode current is varied from 2.2 to 3 kA. It is noteworthy that the tail current varies little with anode current.

Fig. 7 shows the results of the same test as for Fig. 6 but with V\textsubscript{GA} = 20 V. The anode gate unit is now able to eliminate the tail current reducing the turn-off loss from 21 Ws at 3 kA to 8.3 Ws, a 60% improvement (with respect to itself).

The same device as tested in Figs. 6 and 7 is successfully tested to 3.3 kA/2.8 kV in Fig. 8. All the turn-off losses appear to be generated in the voltage-rise and current-fall phases, the tail losses having been virtually eliminated. The device generates a measured loss of 13.5 Ws. The voltage-rise and current-fall times are both 1.4 and 1.6 µs respectively leading to calculated losses during these phases of 6.46 Ws and 7.37 Ws each. Thus the total rise and fall losses are a calculated 13.8 Ws which indeed indicates the absence of a tail current.
C. Comparison with Conventional IGCTs

In Fig. 9, the turn-off waveforms of two differently irradiated standard IGCTs of 4.5 kV rating are compared with those of a 5.5 kV dual-gate device when synchronously gated ($\Delta t = 0$ $\mu$s) and when pre-triggered with $\Delta t = 1.5$ $\mu$s. Although the 5.5 kV device has a 20% thicker n-base, the comparison is made because, as a symmetrically structured device, it has a similar on-state voltage to one of the two asymmetrically structured IGCTs (2.55 and 2.61 V @ $I_A = 4$ kA, $T_j = 125^\circ$C for the 5.5 kV dual-gate and one of the 4.5 kV IGCTs respectively). Additionally, they have similar turn-off losses (about 10 Ws) in the case of the synchronously triggered dual-gate. Pre-triggering the dual-gate device by 1.5 $\mu$s reduces $E_{OFF}$ by 30% to 7 Ws. Further pre-triggering is not possible as the anode current falls faster than linearly and provokes a “snap-off” as it goes to zero resulting in a high peak voltage ($\approx 5.5$ kV). Correcting the 30% loss improvement to allow for the thicker silicon used results in an effective improvement of 44%
In a repetition of the experiment of Fig. 9, the anode current was lowered from 2.8 kA to 2.4 kA and the pre-trigger advanced to 2 µs before the over-voltage also reached 5.5 kV. This resulted in a 36% loss reduction or 49% corrected which was the best improvement, with respect to a conventional IGCT, obtained in the present series of experiments.

In Fig. 10, a low on-state IGCT is compared with a 4.5 kV Dual-Gate IGCT of similar on-state and silicon thickness. In this test, the on-set of snaph occurred at Δt = 0 µs for 2.8 kV and 3.3 kA. With the synchronous triggering used, only 18% loss reduction was achieved. The tail current was eliminated but the bulk of the losses were located in the rise and fall phases rendering the gate-assisted turn-off of little value.

D. Discussion of the Measurement Results

Figs. 6 to 10 illustrate that the symmetric design allows very low on-state devices to be realized. The turn-off losses are effectively reduced by pre-triggering where:

- the silicon is thicker: Fig. 10 (18% improvement) vs Fig. 9 (30% improvement)
- the current is lower: (2.8 kA - 30% improvement) vs. (2.4 kA - 36% improvement)
- maximum pre-triggering can be exploited without snap.

Fig. 9 shows that higher voltage devices (5.5 vs. 4.5 kV) can be made with the same on-state voltage (2.55 - 2.61 V at 4 kA/125°C) while still achieving a 30% loss reduction at 2.8 kV DC. Alternatively, the same turn-off losses and on-state voltages should be achieved at 3.6 kV DC (30% voltage increase).

Fig. 11 shows the turn-off waveforms of conventional 4.5 kV IGCTs with three different irradiation levels [6].

Fig. 9. Comparison of two IGCTs type 5SHY 35L4510 (different irradiation doses) with a 5.5 kV Dual-Gate device @ 2.8kV/2.8kA, Tj = 85°C, VGa = 20V  1) IGCT, VTm = 2.23 V  2) IGCT, VTm = 2.61 V  3) Dual-Gate IGCT,  4) Dual-Gate IGCT VTm = 2.55 V, Δt = 0 µs, VTm = 2.55 V, Δt = 1.5 µs

Fig. 10. Comparison of two IGCTs, type 5SHY 35L4510 4.5 kV standard IGCT with a 4.5 kV Dual-Gate IGCT @ 2.8kV/3.3kA/85°C IGCT, VTm = 2.23 V@ 4kA (pronounced tail) Dual-Gate IGCT, VTm = 2.10 V@ 4kA, Δt = 0 µs, VGa = 20V (no tail)

Lifetime control (by irradiation) effects all three phases of the snubberless turn-off process:

Phase 1 - rising voltage at constant current
Phase 2 - falling current at (approx.) constant voltage
Phase 3 - tail current at (approx.) constant voltage.

The effect of de-saturating the anode pnp transistor prior to and during turn-off has been shown to completely eliminate the Phase 3 tail current losses. Advancing pre-triggering also has an action on the Phase 2 falling current at constant voltage, causing the anode current to fall so rapidly that over-voltage spikes are generated which ultimately exceed the device’s blocking capability. This explains why the greatest
loss-reduction benefits are achieved with the longest lifetime devices as these have the largest tail currents. Pre-triggering is limited by the on-set of snap-off. Snap is aggravated by thin silicon and high currents indicating that this technology will be of benefit at the higher voltages and their correspondingly lower currents.

The first measurements performed on transparent emitter devices (Figs 4 and 5) showed no tendency to snap even with $\Delta t$ of 6 $\mu$s. Furthermore, the $E_{\text{OFF}}$ reduction resulting from reducing tail current with increasing pre-trigger was partly off-set by a “prematurely rising” anode voltage. This is clearly not the case with a high sensitivity to pre-triggering.

The conventional IGCTs shown in Fig. 11 exhibit peak values of $dv/dt$ between 2 and 6 kV/$\mu$s and of $di/dt$ between 2 and 4 kA/$\mu$s. These appear to be application-acceptable values for EMC considerations. Efforts should be made to achieve shorter rise and fall times through anode-gate control (while controlling snap-off) if the ambitious goal of a factor 3 $E_{\text{OFF}}$ reduction is to be achieved. Otherwise, a factor 2 improvement with current techniques is feasible.

Simulations of 10 kV conventional IGCTs [1] have shown that allowing the turn-off loss of a 91 mm device to double results in a 50% reduction of on-state voltage (see Fig. 12). Realizing a dual-gate 10 kV device with an on-state voltage of about 2.6 V at 2100 A instead of the simulated 5.3 V would correspond to a device having 20 Ws loss switching 2.1 kA against 5.1 kV – the same loss as currently achieved by 4.5 kV IGCTs switching 4 kA against 2.8 kV and having on-state voltages of 2.7 V at 4000 A.

IV. CONCLUSIONS

The use of an anode gate can eliminate the tail current of the conventional IGCT. In this respect, it is even more effective than lifetime control, which only reduces tail-losses while increasing conduction losses. Anode-gate control also offers the possibility of reducing rise and fall times (which has now become the dominant switching loss).

The symmetric structure is found to offer the greatest loss reductions and to allow even lower on-states than achieved by the transparent emitter of conventional IGCTs.

REFERENCES


