Practical Medium Voltage Converter Topologies for High Power Applications

Peter K. Steimer
R&D Drives & Power Electronics
ABB Industrie AG
5300 Turgi, Switzerland
E-mail: peter.steimer@ch.abb.com

Madhav D. Manjrekar
R&D Power Electronics Systems
ABB Industrial Systems,
New Berlin, WI 53151-2858, USA
E-mail: madhav.manjrekar@us.abb.com

Abstract- Multilevel power conversion has been receiving increasing attention in the past few years for high power applications [1]. Numerous topologies and modulation strategies have been introduced and studied extensively for utility and drive applications in the recent literature. These converters are suitable in high voltage and high power applications due to their ability to synthesize waveforms with better harmonic spectrum and attain higher voltages with a limited maximum device rating. Trends in power semiconductor technology indicate a trade-off in the selection of power devices in terms of switching frequency and voltage sustaining capability. New multi-level, high power converter topologies have been proposed using a hybrid approach involving Integrated Gate Commutated Thyristors (IGCT) and Insulated Gate Bipolar Transistors (IGBT) operating in synergism. This paper is further developing and optimizing this approach presenting a hybrid nine-level inverter operating at a 4160 V system voltage. Excellent current and voltage waveforms can be achieved even in weak network conditions. Additionally it is shown, that the multi-level conversion system can further be simplified by utilizing series connected H-bridges without the need of supply transformers and rectifiers.

I. INTRODUCTION

Multilevel power conversion has been receiving increasing attention in the past few years for high power applications [1]. Numerous topologies and modulation strategies have been introduced and studied extensively for utility and drive applications in the recent literature. These converters are suitable in high voltage and high power applications due to their ability to synthesize waveforms with better harmonic spectrum and attain higher voltages with a limited maximum device rating.

In the family of multilevel inverters the three-level topology, called Neutral Point Clamped (NPC) inverter, is one of the few topologies that has received a reasonable consensus in the high power community [2]. These NPC inverters have also been implemented successfully in the industrial applications for high power drives [3]. A simplified schematic of a medium voltage drive based on a NPC inverter and a photograph of its industrial implementation is presented in Figures 1 and 2.

Figure 1: Simplified schematic of the industry-standard medium voltage drive based on NPC inverter.
link. By closing two of the four switches, the load can be either connected to the top, middle or bottom of the dc link, thereby generating a three-level voltage waveform at the phase leg output. The LC sine filter connected at the output is used to filter out the high frequency switching components in the output voltage. The dc link capacitors are charged with a twin diode-bridge rectifier configuration. The \( \Delta/Y/\Delta \) phase-shifting transformer feeding the diode bridges generates a twelve-pulse current waveform at the utility side. This transformer also converts the utility voltage to needed input voltage level.

II. NPC-INVERTER AND PASSIVE FILTER

The NPC medium voltage power circuit, including sine filter, as shown on the motor side, could also be used on the line side to serve as an active rectifier unit for high power industry (MV drives) and utility applications (interties, static VAr compensators).

A simplified schematic of such a active rectifier topology, employed on the utility interface side, is shown in Figure 3.

As shown in Figure 3, the output of the NPC inverter is directly connected through an LCL filter to the 4160V utility network. Optionally the utility side reactor can be replaced by a feeder transformer which adjusts to higher utility voltages by employing an appropriate turns-ratio. The voltages on the dc link capacitors are maintained at their nominal values by drawing necessary real power from the utility. One of the primary concerns for a successful operation is meeting the harmonic requirements given by IEEE 519-1992 even at very low short-circuit ratio. Hence, the LCL filter connected at the output of the inverter needs to be adequately sized as to meet the stringent current and voltage requirements. At multi-megawatt power levels, where inherently lower short circuit ratios are existing, the dimensioning of such filters becomes a important issue.

To meet the IEEE 519 limits by means of an NPC inverter and an optimally sized filter the approach of optimized pulse patterns is used. By means of optimized pulse pattern low order harmonics are eliminated by the converter and the remaining high order harmonics are eliminated by the passive filter.
To calculate the optimised pulse pattern the investigation is started with the following basic waveform (see Figure 4):

![Basic waveform](image)

**Figure 4: Basic waveform for optimised pulse pattern investigations**

This waveform can be represented by means of its harmonic content as follows:

\[
U(\phi, t) = \frac{4}{\pi} \frac{U_d}{2} \sum_{n=1,3,5,...} \frac{1}{n} \sin(n \cdot \frac{\pi}{2}) \cdot \left[ \cos(n \cdot (\omega t + \varphi)) + \cos(n \cdot (\omega t - \varphi)) \right]
\]

Based on this equation the basic equation for a waveform with multiple notches can be defined. The angles for a pattern with eight notches per half period, defined by nine free selectable switching angles is therefore defined as follows:

\[
U(\varphi_{11}, \varphi_{12}, \varphi_{21}, \varphi_{22}, \varphi_{31}, \varphi_{32}, \varphi_{41}, \varphi_{42}, \varphi_{51}, t) = \frac{4}{\pi} \frac{U_d}{2} \sum_{n=1,3,5,...} \frac{1}{n} \sin(n \cdot \frac{\pi}{2}) \cdot \left[ \cos(n \cdot (\omega t + \varphi_{11}) + \cos(n \cdot (\omega t - \varphi_{11})) \right] + \\
- \left[ \cos(n \cdot (\omega t + \varphi_{12}) + \cos(n \cdot (\omega t - \varphi_{12})) \right] + \\
+ \left[ \cos(n \cdot (\omega t + \varphi_{21}) + \cos(n \cdot (\omega t - \varphi_{21})) \right] + \\
- \left[ \cos(n \cdot (\omega t + \varphi_{22}) + \cos(n \cdot (\omega t - \varphi_{22})) \right] + \\
+ \left[ \cos(n \cdot (\omega t + \varphi_{31}) + \cos(n \cdot (\omega t - \varphi_{31})) \right] + \\
- \left[ \cos(n \cdot (\omega t + \varphi_{32}) + \cos(n \cdot (\omega t - \varphi_{32})) \right] + \\
+ \left[ \cos(n \cdot (\omega t + \varphi_{41}) + \cos(n \cdot (\omega t - \varphi_{41})) \right] + \\
- \left[ \cos(n \cdot (\omega t + \varphi_{42}) + \cos(n \cdot (\omega t - \varphi_{42})) \right] + \\
+ \left[ \cos(n \cdot (\omega t + \varphi_{51}) + \cos(n \cdot (\omega t - \varphi_{51})) \right]
\]

Result after using goniometric equations to separate each harmonic:

\[
U(\varphi_{11}, \varphi_{12}, \varphi_{21}, \varphi_{22}, \varphi_{31}, \varphi_{32}, \varphi_{41}, \varphi_{42}, \varphi_{51}, t) = \frac{4}{\pi} \frac{U_d}{2} \sum_{n=1,3,5,...} \frac{1}{n} \sin(n \cdot \frac{\pi}{2}) \cdot \\
\left[ 2 \cdot \cos(n \cdot \varphi_{11}) \cdot \cos(n \cdot \omega t) \right] + \\
- \left[ 2 \cdot \cos(n \cdot \varphi_{12}) \cdot \cos(n \cdot \omega t) \right] + \\
+ \left[ 2 \cdot \cos(n \cdot \varphi_{21}) \cdot \cos(n \cdot \omega t) \right] + \\
- \left[ 2 \cdot \cos(n \cdot \varphi_{22}) \cdot \cos(n \cdot \omega t) \right] + \\
+ \left[ 2 \cdot \cos(n \cdot \varphi_{31}) \cdot \cos(n \cdot \omega t) \right] + \\
- \left[ 2 \cdot \cos(n \cdot \varphi_{32}) \cdot \cos(n \cdot \omega t) \right] + \\
+ \left[ 2 \cdot \cos(n \cdot \varphi_{41}) \cdot \cos(n \cdot \omega t) \right] + \\
- \left[ 2 \cdot \cos(n \cdot \varphi_{42}) \cdot \cos(n \cdot \omega t) \right] + \\
+ \left[ 2 \cdot \cos(n \cdot \varphi_{51}) \cdot \cos(n \cdot \omega t) \right]
\]

Derived general definition of the amplitude of the n\textsuperscript{th} harmonic:

\[
\hat{U}_n = \frac{4}{\pi} \frac{U_d}{2} \frac{1}{n} \sin(n \cdot \frac{\pi}{2}) \cdot \\
\left[ 2 \cdot \cos(n \cdot \varphi_{11}) \right] + \\
- \left[ 2 \cdot \cos(n \cdot \varphi_{12}) \right] + \\
+ \left[ 2 \cdot \cos(n \cdot \varphi_{21}) \right] + \\
- \left[ 2 \cdot \cos(n \cdot \varphi_{22}) \right] + \\
+ \left[ 2 \cdot \cos(n \cdot \varphi_{31}) \right] + \\
- \left[ 2 \cdot \cos(n \cdot \varphi_{32}) \right] + \\
+ \left[ 2 \cdot \cos(n \cdot \varphi_{41}) \right] + \\
- \left[ 2 \cdot \cos(n \cdot \varphi_{42}) \right] + \\
+ \left[ 2 \cdot \cos(n \cdot \varphi_{51}) \right]
\]

This basic equations to describe the harmonics have been used to calculate the optimised pulse pattern, with the target of controlling the fundamental voltage and eliminating the 5\textsuperscript{th}, 7\textsuperscript{th}, 11\textsuperscript{th}, 13\textsuperscript{th}, 17\textsuperscript{th}, 19\textsuperscript{th}, 23\textsuperscript{rd} and 25\textsuperscript{th}.

In Figure 5 the switching angles are shown for a modulation index range from of 0.91 (which is the point of operation with 10% utility undervoltage) upto 1.11 (which is the point of operation with 10% utility overvoltage). The nominal point of operation is assumed to be at a modulation index of 1.01. The maximum possible modulation index is 1.14, which assumes, that appr. 3% are available as control margin.
Figure 5: Optimised switching angles as a function of the modulation index for elimination of the 5\textsuperscript{th}, 7\textsuperscript{th}, 11\textsuperscript{th}, 13\textsuperscript{th}, 17\textsuperscript{th}, 19\textsuperscript{th}, 23\textsuperscript{rd} and 25\textsuperscript{th} harmonics

This results in the following half DC voltage level for a 4160V output voltage:

\[ U_{dc\_igct\_N} = \frac{1}{\text{mod}_{N}} \cdot \frac{4160V \cdot \sqrt{2}}{\sqrt{3}} = 3365Vdc \]

which has been the base for all the calculations.

Figure 6: NPC inverter voltage waveform (red) and utility current waveform (blue) with passive filter

For the dimensioning of the sine filter the following points have to be considered:

- The reactor on the inverter side is defined in such a way, that the inverter ripple current remains acceptable.
- The utility side reactor should be selected to sufficiently limit any short-circuit currents.
- The filter capacitor is selected in such a way, that the resonance frequency stays close to nine times the fundamental in every operation point.

By means of the presented solution based on the combination of a NPC inverter, switching with a frequency corresponding to a PWM carrier close to 1kHz, and a passive filter the IEEE 519 requirements can be met. The total harmonic distortion of the utility current will in practice be in the range of 1.5 to 2\%. See Figure 6 and 7.

Figure 7: Utility current harmonics at the utility side meeting IEEE 519 requirements (SCR < 20)

Figure 8: Utility voltage harmonics meeting IEEE 519 requirements (SCR < 20). Total THD less than 1\%.

In the case of a weak grid, as assumed in the investigations with a short-circuit ratio of 20, the voltage distortion seen at the utility connection is of
interest too. The corresponding results for a SCR of 20 is shown in Figure 8.

The NPC medium voltage IGCT inverter in combination with a passive filter can meet stringent IEEE 519 requirements. In regards of further improvements the elimination of any line-side capacitors (risk of resonance or active resonance control needed) and increased efficiency would be of significant interest.

III. NPC-INVERTER AND ACTIVE FILTER

Basics power semiconductor physics indicate a trade-off in the selection of power devices in terms of switching frequency and voltage sustaining capability [4]. Normally, voltage blocking capability of faster devices such as Insulated Gate Bipolar Transistors (IGBT) and the switching speed of high voltage latching devices such as Integrated Gate Commutated Thyristors (IGCT) [5] is found to be limited. The IGBT has its strength at 600V up to 1700V, with PWM frequencies in the range of multiple kHz. The IGCT, or any other medium voltage semiconductor, has its strength at 4500V up to 6000V with PWM frequencies up to 1kHz.

In Figure 9 a picture of a 6kV/3000A IGCT, the preferred switch for any medium voltage application, is shown. In Figure 10 a picture of a newest generation 1700V / 6 x 240A IGBT (LoPak5), the preferred switch for any low voltage application, is shown.

Therefore the concept of the hybrid inverter is based on the combination of

- a high-power NPC medium voltage IGCT inverter, mainly for power transfer, and
- multiple low-power 2-level (H-bridge), low voltage IGBT inverters, mainly for series active filter tasks.

To minimize the amount of components the hybrid converter, see [6] and [7] and its control strategies [8] have been further developed. As major improvement the supply section (transformer, rectifier) of the series low voltage IGBT inverters has been eliminated. It will be shown, that the voltage of the “flying” low voltage IGBT inverters can be controlled without the need of any additional supply circuit. A simplified schematic of the power circuit of the proposed system is shown in Figure 11.
The equivalent vector space representation of the proposed hybrid multilevel inverter results by superimposing the vector spaces of the small H-bridge inverters (red thin-lined hexagons) on the vector nodes of the big three-level inverter (blue thick-lined hexagon). The corresponding result is shown in Figure 12.

For the following investigations it is assumed, that the DC-links of the series active filters are controlled by their own. The DC-Link of the NPC-inverter is controlled over the main transformer and may be the connection point for any other loads, i.e. the motor-side NPC-inverter of a medium voltage drive as shown in Figure 1. The DC link voltages of such a hybrid converter systems are configured in a 3:1 ratio (half NPC-voltages versus H-bridge voltages). To get the system running without any supply on the low voltage IGBT inverters, it has to be avoided, that any real power has to be transferred over the series IGBT inverters. This means, that in average all real power has to be transmitted over the larger NPC medium voltage IGCT inverter. To achieve this the DC-link voltage of the IGCT inverter has to be set high enough. The proposed DC-link voltages for the NPC inverter (half DC link voltage) and for the H-bridges are as follows:

\[ U_{dc \_igct } = 3000\text{Vdc} \]
\[ U_{dc \_ibgt } = 1000\text{Vdc} \]

Because the relevant DC-link voltage available to generate the needed output voltage is the sum of the NPC inverter voltages (3000 Vdc) and the IGBT inverter voltage (1000Vdc), this topology reduces actually the DC voltage requirements for the NPC medium voltage IGCT inverter (from 33365Vdc down to 3000Vdc) and requires a DC link voltage of 1000Vdc for the series 2-level 1700V IGBT inverters. The proposed hybrid approach therefore realizes a multilevel inverter using IGCTs and IGBTs operating at the optimal DC-link voltages in synergism.

In Figure 13 and 14 the hybrid modulation concept is shown for the nominal operation point with a modulation index of 0.85, referenced to 4000Vdc, with a carrier frequency of 39 times the fundamental frequency.
This selection of the DC link voltages and the 3:1 ratio allows the realization of a 9-level inverter with the targeted benefits, that the passive filter can be eliminated and no supply for the active filter bridges is needed. Using appropriate modulation strategy, it will be possible to synthesize stepped waveforms with voltage levels -4kV, -3kV, -2kV, -1kV, 0, +1kV, +2kV, +3kV, +4kV using only one three-level inverters combined with 3 H-bridge converters, in total 24 power semiconductors.

To control the DC-link voltages of the floating series IGBT inverters the 3rd harmonic included in the reference signal used for the modulation has to be controlled accordingly. By this simple means the hybrid converter system without supply of the IGBT DC-link can be controlled in a robust manner.

If utilized in connection with a weak utility connection the interest in regards of created voltage distortion at the point of connection is increasing. In this respect the hybrid converter solution with the selected carrier frequency results in total THD for the utility voltage at the PCC of less than 3% at a SCR = 20. With this modulation concept of the hybrid inverter a THD of the utility current of appr. 2-3% will be achieved in practice (utility interfacing inductance = 0.12p.u.).

By increasing the carrier frequency, the THD of the utility current can be further improved and the voltage harmonics at the point of common coupling can be moved to higher frequencies. If this higher harmonics in the utility voltage should be further reduced, this can easily be done by installing small RC circuits at the utility side of the utility interfacing inductance to create a high frequency, passive filter.

The operation of the hybrid converter has been verified by laboratory tests [7] and by means of detailed system simulations. In Figure 17 the achieved results with a carrier frequency of \( f_c = 39 \times f_1 \) are shown. As can be seen, the capacitor voltage of the IGBT inverter (see \( u_{\text{IGBT}} \)) stays constant, without any supply.
IV. CONCLUSIONS

Based on the shown performance it can be concluded, that with the hybrid converter system

- based on a powerful IGCT NPC-inverter
- based on a series active filters realized by one IGBT H-bridge inverter per phase
- without any supply of the series active filters

a competitive line-friendly concept has been presented.

It has been shown, that the hybrid converter system based on a NPC inverter with medium voltage power semiconductors (i.e. 6kV IGCTs) and with series IGBT inverters with low voltage IGBTs (i.e. 1700V IGBTs) can be controlled in such a manner, that
- IEEE 519 requirements can be met,
- low distortion of the utility voltage even in case of a weak grid can be achieved,
- the supply infrastructure for the series IGBT converters can be avoided and
- an excellent efficiency can be achieved.

TABLE I: Comparison of topologies

<table>
<thead>
<tr>
<th>SCR</th>
<th>I_THD</th>
<th>U_THD</th>
<th>f_pwm</th>
<th>η</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>[1]</td>
<td>[1]</td>
<td>[2]</td>
<td>[3]</td>
</tr>
<tr>
<td>NPC inverter and passive filter</td>
<td>1.5-2%</td>
<td>&lt; 1.2%, IGCT: 1080 Hz</td>
<td>Appr. 98.7%</td>
<td></td>
</tr>
<tr>
<td>NPC inverter and series active filter without supply</td>
<td>2-3%</td>
<td>&lt; 3%</td>
<td>IGCT: 600 Hz, IGBT: 2760 Hz (with f_carr = 39xf1)</td>
<td>Appr. 99.2%</td>
</tr>
</tbody>
</table>

Remarks:
1) THD include sum up to the 100th harmonic, realistic values are given including control and limited DC-link energy storage influence.
2) As PWM frequency a number corresponding to the maximum device stress is given.
3) Losses of utility side inductance (transformer) not included

REFERENCES