

SOA in High Power Semiconductors

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SOA in High Power Semiconductors

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Abstract — This paper gives an overview on the SOA of high power semiconductors. Two main types of high power semiconductors are investigated: large area devices and modules with paralleled chips. The paper explains the limits of SOA and ways of improving it in the semiconductor design level, as well as it gives practical advantages for a high SOA in the device.

Keywords-component; Safe Operating Area; SOA; IGBT; IGCT; high power semiconductor

I. INTRODUCTION

One of the main challenges today in the design of high voltage – high power semiconductors is the Safe Operating Area “SOA” capability [1]. A destruction point characterizes the SOA limits whereas failures are largely related to the device design and/or process. In recent years, the SOA performance for medium to low voltage devices has improved immensely. Optimized emitter cell designs, the introduction of the NPT and SPT vertical design concepts in IGBTs and better-controlled lifetime reduction techniques have all helped in this direction. However, previous experience and literature has clearly pointed out that the SOA performance for higher voltage devices rated above 2000V degrades significantly when compared to the low to medium voltage class devices. This downtrend is due to physical constraints in high voltage structures and the high stress operating conditions. Furthermore, the trade-off between the optimisation of the overall losses and the SOA capability has imposed further restrictions in the design window of high voltage semiconductors.

The paper is structured as two parts. First part will investigate the SOA in large area devices (eg. GCT, GTO, etc.) and the second part focuses on the IGBT modules which consist of paralleled chips.

II. TRENDS IN SOA

Trends for the development of power semiconductors aimed for wide SOA limits are fuelled by many requirements in applications operating under hard-switching conditions. Evolution of SOA for an improved safe operating area is demonstrated in Fig. 1.

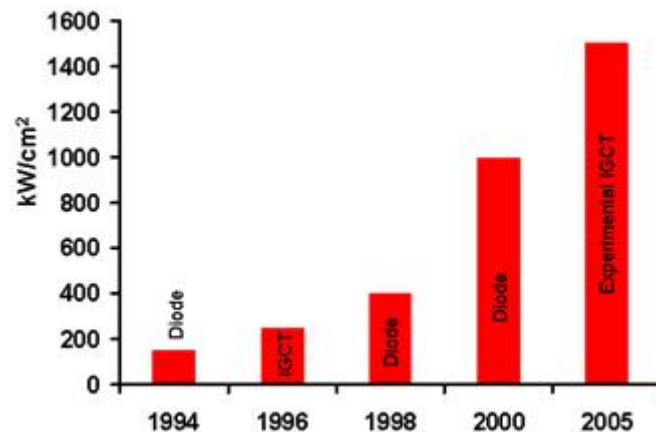


Figure 1. Evolution of SOA

Improved SOA performance will have a positive impact on

- i. manufacturability,
- ii. reliability,
- iii. power handling capability,
- iv. ease of paralleling,
- v. better controllability,
- vi. better system and gate drive designs aimed at reducing the total system losses, and
- vii. employing more optimised protection schemes.

In order to ensure that high voltage devices do not exceed their SOA limits, many restrictions were introduced for operating such devices. Therefore, system designers have resolved into setting many circuit and gate drive parameters accordingly. Such modifications include an increase in gate resistance and the inclusion of protective active clamps or snubbers. This added complexity has had normally a negative impact on the performance, cost and size of high power electronic systems.

In order to overcome these problems, larger SOAs are always favorable by the system designers and applications engineers and for that reason semiconductor manufacturers have always felt the pressure for designing better SOA performance devices. The new limits are reached by introducing new technologies in the power semiconductor designs as shown in Fig. 2.

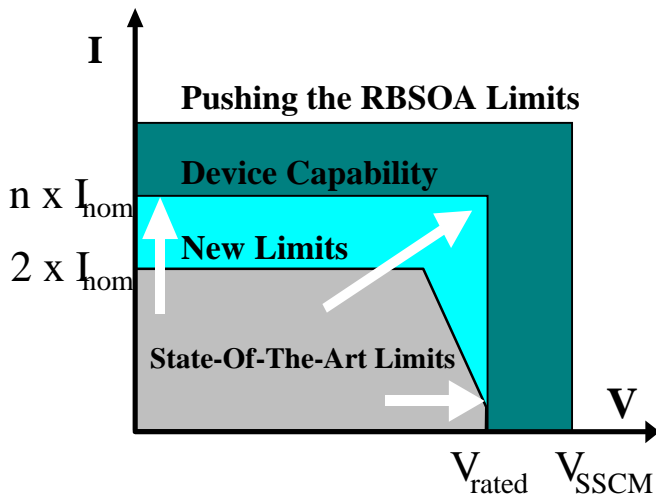


Figure 2. Extending the RBSOA limits of HV Power Semiconductors

III. INCREASED SOA IN LARGE AREA DEVICES
- A CASE FOR IGCT-

Previous experience and data have shown that the SOA of high voltage devices up to 6500V degrades due to the physical stresses at very high voltage. Although improvements in SOA have been achieved, the turn-off capability of large area IGCT devices is still the main parameter limiting higher system ratings, especially at low temperatures.

The IGCT consists of a large number of parallel-operated thyristor cells (Fig. 3) driven by a single gate unit. SOA performance can be limited by the following factors:

- i. ruggedness of the individual cell
- ii. current sharing effects due to heavy paralleling of the cells [2]
- iii. performance of the gate-driver [3, 4].

Analysis of the SOA limits for large area IGCTs has led to the following observations:

- a larger active area of an IGCT always results in a lower average switching power density, even when accounting for the scaling of the switching circuit,
- an increase by a factor of 10 in active area only leads to an increase in turn-off current capability of a factor of four,
- the SOA limit of a large area IGCT is typically reached while still operating in the macroscopic hard switching regime (i.e. the current commutation from cathode to gate is completed before the anode voltage starts to rise),
- SOA failures are typically found in areas remote from the gate contact.

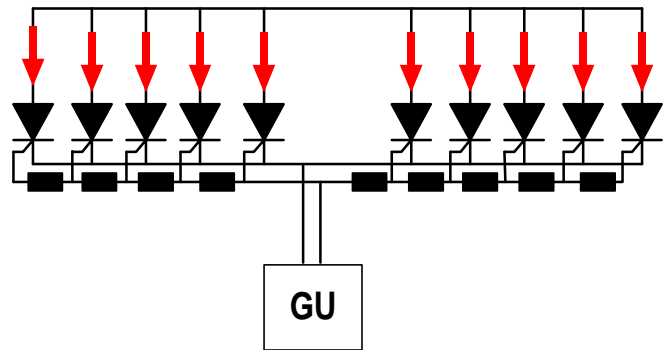


Figure 3. Principal of IGCT operation as parallel connected thyristor cells with an attached gate unit

Based on these findings, the improvement of the SOA performance was carried out in three steps: cell optimization (local SOA), lateral optimization of large area devices and a combination of local and lateral optimization techniques.

A. Cell Optimization

The improvement of the cell design by optimizing doping profiles resulted in a maximum switching power density of 1.5MW/cm² for snubberless operation even when scaling up the clamp stray inductance to 9.1μH for a device with 1.5cm² active area (Fig. 4). Here the ‘Switching-Self-Clamping-Mode’ (SSCM) could be seen for the IGCT when switched against a high DC-voltage and high clamp stray inductance. The SSCM phenomena will be explained in the next section in detail.

B. Lateral Optimization of Large Area Devices

A large area IGCT’s SOA was found to be significantly below the switching power density of small devices. Therefore, it must be concluded that a current redistribution during device turn-off is taking place. The major observation that failure locations are remotely located from the gate contact leads to the logical conclusion that the current redistributes into these remote areas during turn-off. Tailoring the current density distribution during the on-state phase by means of local charge carrier lifetime control will reduce the effects of the areas that are limiting the SOA performance of an IGCT. By irradiating the device in remote areas from the gate with a higher electron dose, the local charge carrier lifetime is decreased. By gradually increasing the additional irradiation dose in remote areas, the current turn-off capability increases until an optimum level is reached.

C. Combined Local and Lateral Improvement

These two combinations were proven to have a linear increase in turn-off capability. An increase of SOA of more than 30% at RT (Fig. 5) was observed.

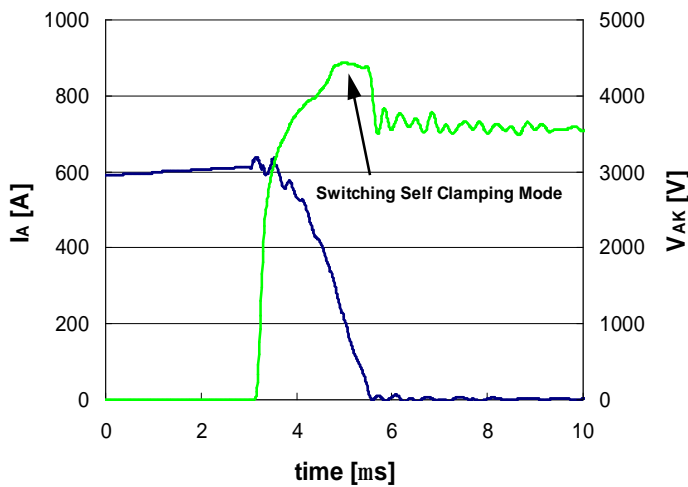


Figure 4. Turn-off characteristic of locally optimized Ø38mm reverse conducting IGBT

device failure. Protection of the N+ source region is vital for increasing the cell latch-up immunity of IGBTs.

Diodes are also limited in their SOA due to dynamic avalanche during reverse recovery. Under the adverse combination of high commutating di/dt, high current densities and high temperatures, the diode is forced during reverse recovery into dynamic avalanche. Extra carriers are then generated that are sensitive to any non-uniformities in the device structure leading to destructive current filaments forming in the device. Optimisation of the diode termination design, process and lifetime control has reduced the risk of filaments occurring during dynamic avalanche resulting in stable reverse recovery performance [5].

B. SOA Improvement Techniques

For high voltage devices with typical low background doping concentrations, the removal of the electron-hole plasma during device turn-off forces the device into a strong dynamic avalanche mode at much lower currents when compared to lower voltage devices. Therefore, limiting substantially the SOA performance of high voltage IGBTs and diodes. We will show in this paper that all typical dynamic avalanche failure modes caused by the removal of the electron-hole plasma can be eliminated. Thereafter, this has led to the device experiencing a self-clamp avalanche mode during turn-off similar to that obtained in a standard unclamped inductive test. We refer to this as the Switching Self-Clamping Mode (SSCM), where the device overshoot voltage reaches a value VSSCM close to the static breakdown voltage of the device as shown in Fig. 6.

As the voltage rises, the IGBT goes into dynamic avalanche immediately after the MOS channel ceases to inject electrons into the n-base region. The lack of electron compensation for the recovering holes will modify the effective background doping and electric field distribution characterised by the lower dv/dt value during dynamic avalanche. Unless device failure occurs, the dynamic avalanche phase continues until the remaining electron-hole plasma is used up and subsequently dynamic avalanche is suddenly eliminated. Because of the stray inductance in the commutation circuit, the voltage over the IGBT starts to rise and eventually reaches the breakdown voltage of the pn-junction, whereas avalanche-generated carriers will carry the reverse current in the IGBT. Optimum design of the device buffer region by employing a Soft-Punch-Through SPT concept will enable the device to withstand such conditions by self-clamping the overshoot voltage successfully. Thus, leading to an ultimate square SOA capability up to the device blocking voltage.

C. New HV-IGBT design platform

The new technology was developed mainly for increasing substantially the cell latch-up immunity for a wide SOA performance. The main approach was to carefully optimise the IGBT cell pn junction profile while on the other hand, increase the protection level of the N+ source region especially at the weakest point near the MOS channel.

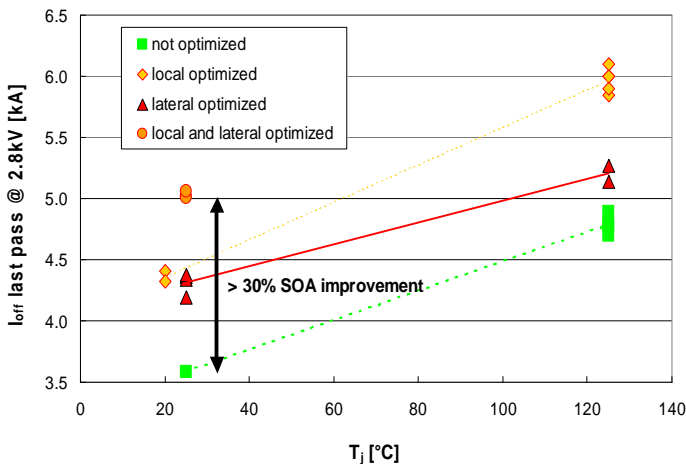


Figure 5. SOA limits (last pass currents for snubberless turn-off at $V_D=2.8kV$, $L_\sigma = 0.3\mu H$) for different junction temperatures and design variations of Ø91mm, 4.5kV, asymmetric GCTs

IV. INCREASED SOA IN DEVICES WITH PARALLELED CHIPS - A CASE FOR IGBT-

In this section, the SOA considerations and improvement techniques in the device level for an IGBT and diode will be explained.

A. Failure mechanisms in IGBT and Diode

Dynamic cell latch-up represents the main failure mode when the IGBT turns off especially under extreme dynamic avalanche conditions. These conditions include high current, high voltage, high temperature, large inductance and low gate resistance values. Failures normally occur when the IGBT N+ source injects enough electrons into the P channel region to cause uncontrolled parasitic thyristor triggering leading to

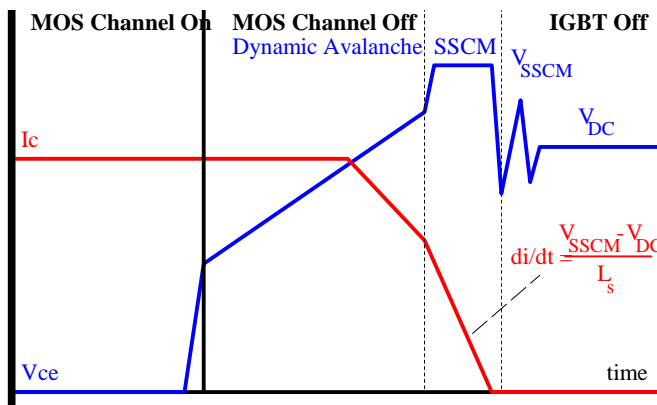


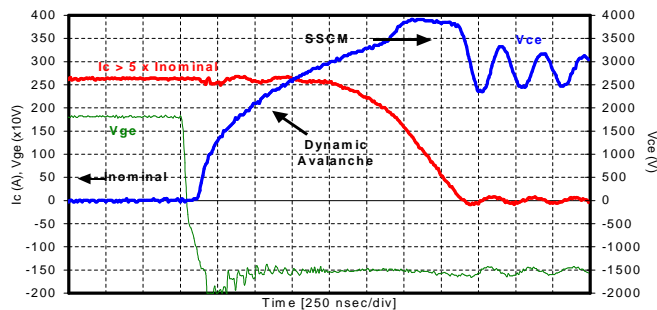
Figure 6. IGBT SOA turn-off waveforms including SSCM

D. New HV-diode design platform

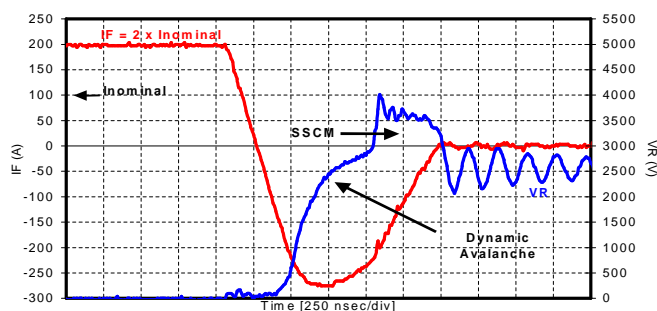
The superior SOA performance of the new HV-diodes was reached by applying a higher doped P+ anode was employed; thus, resulting in an extremely rugged performance when compared to lower P anode diodes. using a combination of local and homogenous lifetime control methods, the electron-hole plasma can be shaped in an optimal way for tailoring the electrical parameters and improve the SOA performance.

E. Test results

In Fig. 7, test results for extreme conditions are given in order to demonstrate the performance of the SSCM technology and thus the improvement in SOA performance on the single chip level.



(a)



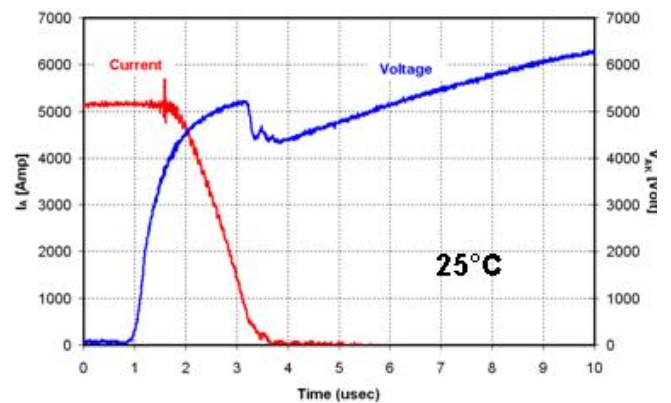
(b)

Figure 7. (a) 3.3kV/50A IGBT Turn-off RBSOA waveforms, (b) 3.3kV/100A Diode Reverse Recovery RBSOA waveforms

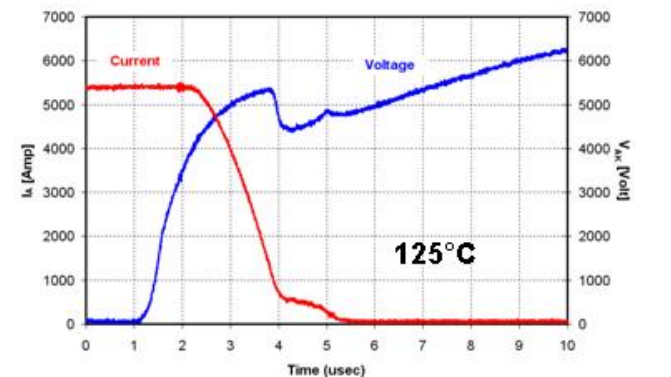
V. EXPERIMENTAL RESULTS

A. IGCT

The improved technology was demonstrated under snubberless conditions on a Ø91mm 6.5kV asymmetric GCT both at room temperature and 125°C as shown in Figure 8.a and 8.b respectively. The device was capable of turning off currents in excess of 5000A at a DC link voltage of 3600V with a peak power dissipation exceeding 20MW for both tests. These results will provide a new outlook for future high voltage applications utilizing high power IGCTs.



(a)



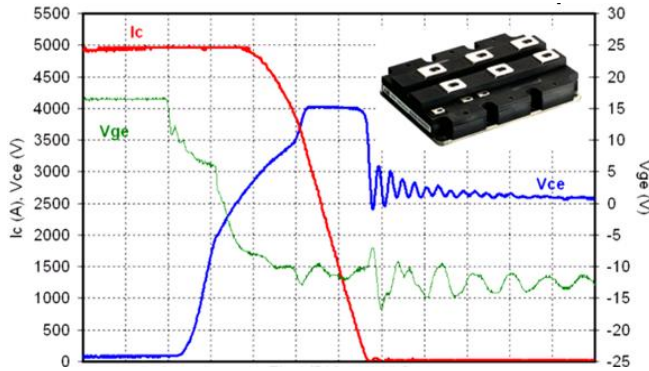
(b)

Figure 8. Optimized vertical design of 91mm/6.5 kV SOA Turn-off waveform of the new Ø91mm 6.5kV asymmetric GCT $V_D=3.6kV, T_J= 25^\circ C, L_s=0.3\mu H$

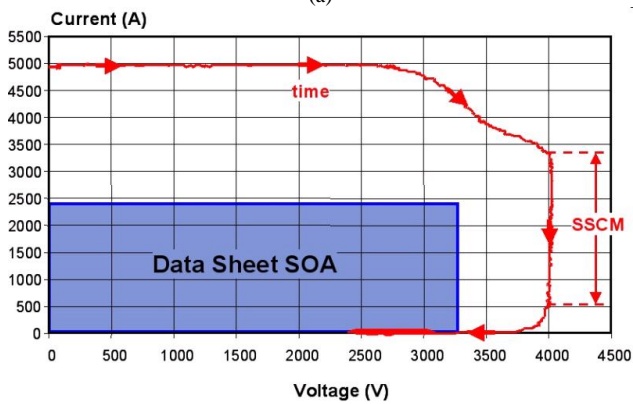
B. IGBT

By enabling the IGBT to withstand SSCM, the device will exhibit a square SOA capability up to the blocking voltage level. This mode of operation can be seen in the 3.3kV/1200A IGBT module RBSOA waveforms shown in Figure 9.a and the associated square SOA I/V curve of Figure 9.b.

The oscillations observed in the current and voltage waveforms (Figure 9.a) after SSCM are a result of the step response to voltage VSSCM – VDC and the oscillatory circuit composed of the high stray circuit inductance and the low device output capacitance during SSCM.



(a)



(b)

Figure 9. (a) 3.3kV IGBT module demonstrating SSCM (0.6 MW/cm²);
 (b) Corresponding SOA
 3.3kV/1200A IGBT module during Turn-off (24 IGBTs)
 V_{cc}= 2600V, I_c= 5000A, R_G= 1.5ohm, L_s= 280nH, T_j= 125°C
Dissipation: 20 J in total, 5 J during self-clamp. 14 MW peak power
 no clamp, no snubbers

VI. CONCLUSIONS

To improve performance and reduce the size and cost of power electronic systems, the development trend in high power semiconductors continues towards higher current and power capabilities. There has always been a pressure on power semiconductor manufacturers, in order to increase the SOA. The presented new benchmark in SOA performances will provide a new outlook for system designers, enabling a far more optimum performance of high voltage power electronics applications.

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