TESTING AND RELIABILITY

4.1 Essentials of Quality and Reliability (Q & R) in Development and Production

The quality and reliability of semiconductors is determined at the design stage; accordingly, these aspects are of primary focus for the development department. Q & R considerations are an integral part of the design and development process as reflected by the *Development Process Model* followed at ABB Semiconductors.

Thus, at each design stage, thorough *Planning for Quality and Reliability* is executed and documented and design results are subject to formal, systematic and critical *Design Reviews* at the conclusion of each design phase.

Verification by appropriate experiments and routine testing according to standardised *Inspection and Test Requirements* are performed in the course of the development cycle. *Design for Reliability* and *Design for Manufacturability* are the main applied concepts and methodologies.

Design for Reliability

ABB Semiconductors strives to address reliability aspects by "proactive engineering" at the early stages of development. This includes:

- use of well documented and standardised process steps;
- use of "predictable" technologies in, for instance, junction termination, doping, passivation etc.;
- adequate safety margins in design rules based on root-cause analysis of failure modes;
- use of state of the art methodology and analytical equipment through co-operation with leading universities and research institutes;
- use of state-of-the-art modelling and simulation tools to compute electrical, thermal and mechanical stresses;
- Failure Mode and Effect Analysis at early stage of development.

High power semiconductors are often used in equipments with extremely long life-expectancies. Examples are locomotives and HVDC valves with life-expectancies of about 30 years. This means that devices must be designed for minimal failure rates and for given projected life-times. The systematic investigation of wear-out mechanisms and the use of wear-out resistant designs and technologies is thus of ut-

most importance. The study of wear-out mechanisms and their modelling often requires special knowledge of materials science which is not universally available. To this effect, ABB Semiconductors relies on ABB Corporate Research and on other leading academic groups.

Design for Manufacturability

A key design goal is to have *one basic process sequence* for each product group (PCT, GTO and Diodes). The main product-to-product variables are then masks, silicon specification, implantation dose, e-doping dose etc. The generic processes, however, remain fixed and standardised (e.g. lifetime control with e-doping only, standardised diffusion temperatures).

Simulation, modelling and statistical tools are used to perform a sensitivity analysis of electrical performance versus process variation in order to define design rules and required process capabilities.

Theoretical cycle time is an important criterion in any new product design. Minimising theoretical cycle time not only brings cost-reductions but also reduces the complexity of process and logistics and increases reliability.

Theoretical yield is maximised by setting specifications such that there is a sufficient margin between typical and limit values. A high theoretical yield is a prerequisite for a stable and predictable production process and thus a necessary condition for product quality and reliability.

4.2 General Production Testing and Device Qualification

The basic test philosophy at ABB Semiconductor (refer to "General Quality Specification for High Power Semiconductors") is based on in-line process control and on four generic test levels:

Group A Testing: – 100% Routine Test for all manufactured devices
Group B Testing: – Lot Control Test (scheduled product audit)
Group C Testing: – Qualification Maintenance Tests (bi-annual)
Group D Testing: – Qualification Approval Test

The in-line control and testing performed during the production sequence of a PCT is described in the following table:

Testing During PCT Manufacturing

Product Category	Un-irradiated Wafer	Classified Wafer	End Product
Production Step	full processing from raw silicon to wafer, testing before irradiation	Irradiation, test and classification of wafer	Assembley, test and classification of end product, marking and gate leading
Type of testing	in-line process control, Group A testing before irradiation	Group A testing for wafer classification	Group A testing for device classification Group B monitoring for lot control test
Related Documents	Product related Run-Sheets and Test Specification before irradiation	Product related Test Specification for wafers	Product related Test Specification for devices
Report	SPC charts, Test Report	Test Report	Test Report

4.3 In-Process Control

The quality of a product is built-in during the manufacturing and assembly stage. The base for each lot run-sheet is a type-generic product flow-chart whereby all operations and control points are specified. Inspection results at the control points are plotted at the station on X/R-charts. This data is the driver for continuous improvement of the process capability. Materials and semi-finished products found out-of-spec are marked and scrapped.

The stage for continuous improvement is set by applying the following tools: *Pareto Analysis, Cause and Effect Analysis, Process Capability Studies, Multi-Vari Analysis, Factorial Experiments and Comparative Experiments.*

Results from the in-process control and final inspection are fed back to earlier processes to improve quality. In-process inspection includes inspections in the wafer fabrication and assembly.

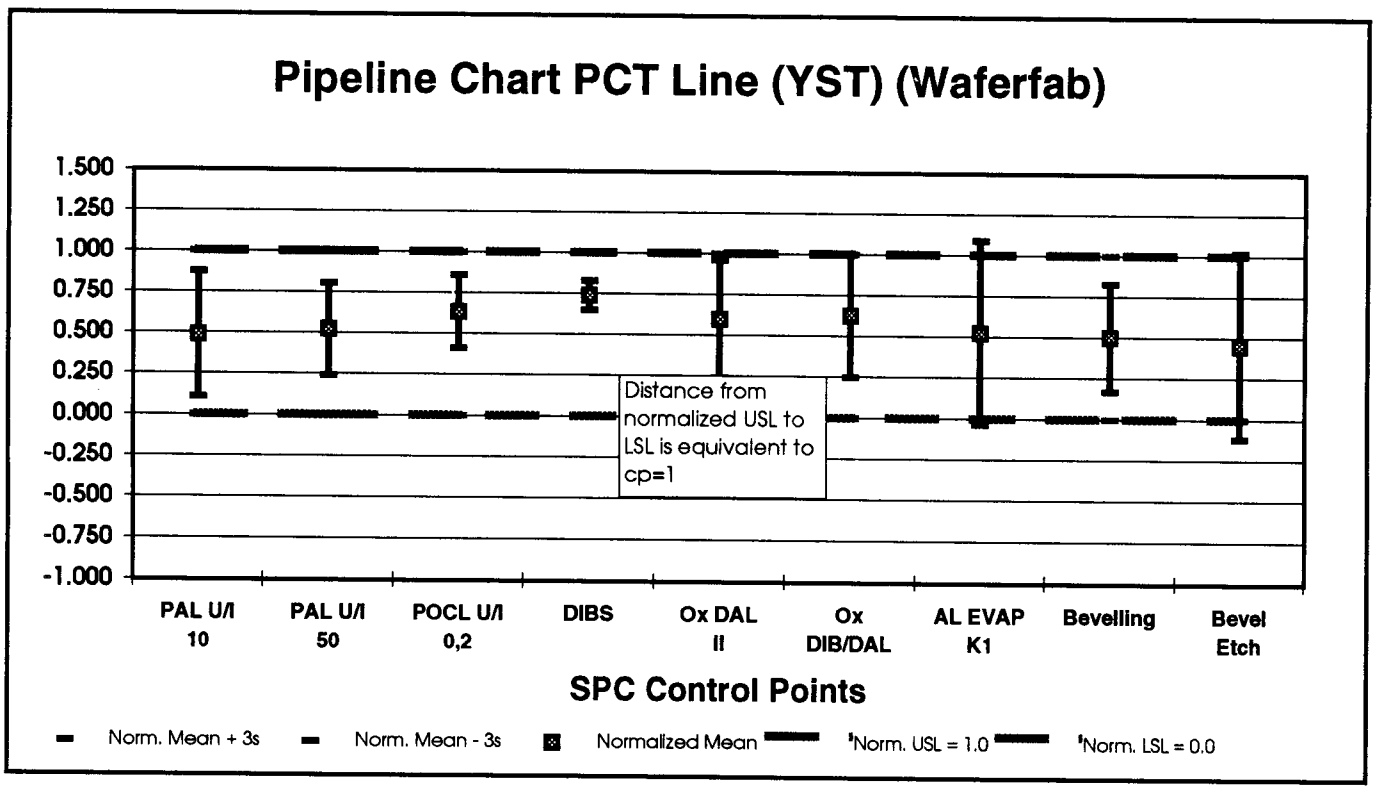
In-Process Inspection Requirements

The following table shows the most important manufacturing steps and the corresponding SPC measurement and/or monitors:

Process Steps	In-Process Inspections/Monitors
Oxidation	– visual – thickness
Photolithography	– mask and wafer cleanliness – alignment and focusing accuracy – critical dimensions
Etching	– quality of etching and wafer cleanliness – critical dimensions
Doping by Diffusion	– sheet resistance
Metallization	– wafer cleanliness – thickness – visual
Passivation	– wetting – passivation integrity (pores) – adjustment
Edge contour	– critical dimensions
Wafer Inspection	– visual (microscope surface inspection)

In-line PCT Control

SPC measurement results and process capability indices for all *Critical-to-Quality* parameters are displayed as monthly Pipeline Charts, in order to indicate the control status of the manufacturing processes.



4.4 Electrical Production Testing

Electrical parameter testing is performed at the wafer level (before and after irradiation) and after packaging (standard or customised final test procedure).
Quality assurance tests include lot control and periodic tests (Group-B testing). For these tests, the acceptance or rejection criteria are device specific. Quality assurance tests include optical inspection and electrical characteristics, as well as thermal, mechanical and operating life (endurance) tests. As for periodic tests, samples are routinely taken for reliability evaluation.

4.4.1 Group A Testing: 100 % Routine Production Testing

Testing of wafer before electron irradiation
Parametric tests prior to electron irradiation are:

Parameter	Temperature	Type of test	Protocols	Remark
Q	125 °C	100%	Test report	determines irradiation dose
V_{RRM}	25	sample test	Test report	
V_{DRM}	25	sample test	Test report	

Testing and classification of wafer after Electron Irradiation
The electrical tests for an irradiated wafer are:

Parameter	Temperature	Type of test	Protocols	Remark
V_{DRM}	25/125 °C	100%	test report	
V_{RRM}	25/125 °C	100%	test report	
V_{DSM}	25/125 °C	100%	test report	for 5200 and 6500 V devices
V_{RSM}	25/125 °C	100%	test report	for 5200 and 6500 V devices
dv/dt crit	125 °C	100%	test report	
Q	125 °C	100%	test report	measured at −1.5 A/µs
V_T	125 °C	100%	test report	
I_{GT}	25/125 °C	100%	test report	
V_{GT}	25/125 °C	100%	test report	
t_q	125 °C	100%	test report	for adapted standards

Turn-off time (t_q) measurements are often required for adapted standard products and these are first tested at wafer level as are other special requirements.
Turn-off time is normally measured at −1.5 A/µs and 20 V/µs. Specific customer requirements for Q_{rr} and t_q at other di/dt and dv/dt conditions are normally correlated per the parametric relations shown in **Section 5** and based on the standard testing conditions above.

Final Device Testing
All devices are finally tested for the following parameters and classified after assembly.

Parameter	Temperature	Type of test	Protocols	Remark
V_{DRM}	25/125 °C	100%	test report	
V_{RRM}	25/125 °C	100%	test report	
V_{DSM}	25/125 °C	100%	test report	for 5200 and 6500 V devices
V_{RSM}	25/125 °C	100%	test report	for 5200 and 6500 V devices
dv/dt crit			test report	the wafer test result
Q			test report	the wafer test result
V_T	125 °C	100%	test report	
I_{GT}	25/125 °C	100%	test report	
V_{GT}	25/125 °C	100%	test report	
t_q			test report	the wafer test result
I_{TSM}	125 °C	100%	test report	for adapted standards

Where I_{TSM} with reapplied voltage is required to be specially tested (adapted standard), this is done at the device level along with any other special tests not listed above.

The Test Reports are the computer print-outs of the final test. Since Q, dv/dt crit and t_q are measured at *wafer level,* these are the values included in the test report where this is required by the customer.
The test sequence and lay-out of the test report for adapted standard products are defined in the *spec. review process* in order to determine the scope of the measurements.

4.4.2 Group B – Lot Control Tests (Scheduled Product Audits)

All other data-sheet values are established during Qualification, Rating and Evaluation (group D testing) into which Group B testing is integrated for final screening. Eight devices per selected lot undergo a voltage stability test for 24 h at V_D, V_R = ⅔ V_{DRM}, V_{RRM}. A typical pass criterion is that the drift of the leakage current be < = 0.2 mA.

Examination or Test		**Reference Documents**		**Inspection Requirements**		
Sub-group	**Test Category**	**IEC Ref.** *MIL-STD-750C Ref.*	**Conditions**	**n**	**c**	**Notes**
B2	Endurance: DC blocking	1048	24 h at T_C = 80 °C ... T_{vj}max V_D, V_R = ⅔ V_{DRM}, V_{RRM}	8	0	

4.5 Qualification Approval Tests and Qualification Maintenance Tests

Every new design undergoes rigorous qualification testing (Group D testing) whereby the data sheet values are verified and the reliability ascertained: this is an essential part of the development model.
Most of these tests are those of the bi-annual reliability monitoring tests (Group C testing). The following table summarises ABB Semiconductors' commitment to reliability.

PCT Qualification Test Procedures

Examination or Test		Reference Documents		Inspection Requirements		
Sub-group	**Test Category**	**IEC Ref.** *MIL-STD-750C Ref.*	**Conditions**	**n**	**c**	**Notes**
D1a	Characteristics inspection	Internal Ref.	Parameters and quantities: see applicable qualification test specification and datasheet			
D1b	Complementary characteristics inspection	Internal Ref.	Parameters and quantities: see applicable qualification test specification and datasheet			
D1c	Verification of maximum ratings	Internal Ref.	Parameters and quantities: see applicable qualification test specification and datasheet			
D2	Endurance: Storage at high temperature	68-2-2 *1031.4*	1000 h at T_{stg} max	10	0	Note 1
D3	Endurance: Storage at low temperature	68-2-1 Aa	500 h at T_{stg} min	10	0	Note 1
D4	Endurance: AC blocking	747-6V	1000 h at $T_C = T_{vj}$ max Sine wave 50 Hz V_D, V_R = ⅔ V_{DRM}, V_{RRM}	8	0	Note 1
D5	Endurance: DC blocking	*1048*	1000 h at T_C = 80 . . . 125 °C V_D, V_R = ⅔ V_{DRM}, V_{RRM}	8	0	Note 1
D6	Endurance: DC blocking	Internal Ref.	1000 h at T_C = 25 °C V_D, V_R = V_{DRM}, V_{RRM} (or derated voltage)	30		Note 1
D7	Endurance: Thermal cycling load (Thermal fatigue)	747-6 IV, 4 *1037.1*	ΔT_{vj} = 80 °C . . . 100 °C $1 \cdot 10^5$ cycles	12	0	Note 1
D8	Endurance: Operating life	Internal Ref.	$1 \cdot 10^6$ on/off cycles with I_{TGQM} and V_D max, specific drive and snubber circuits	10	0	
D9	Rapid change of temperature	68-2-14 Nc *1056.2*	0° C to 100 °C, 15 cycles, liquid to liquid	10	0	Note 1
D10a	Shock	68-2-27 Ea *2016.2*	Components in stack 50 g, 11 ms, 3 shocks per direction	4	0	Note 2
D10b	Vibration	68-2-6 Fc *2056*	Components in stack 20 g, 100 Hz to 2000 Hz, 10 cycles per axis, 90 min	4	0	Note 2
D10c	Shock	68-2-27 Ea *2016.2*	Components in box 50 g, 11 ms, 3 shocks per direction	4	0	Note 2
D11b	Impact Shock (Bump)	68-2-29 Eb	Components in box 40 g, 6 ms, 1000 shocks per direction	4	0	Note 2
D11c	Vibration	68-2-6 Fc *2056*	Components in box 5 g, 10 Hz to 500 Hz, 10 cycles per axis, 120 min	4	0	Note 2
D12	Salt mist	68-2-11 Ka *1046.2*	35 °C, 5% NaCl, 7 days	4	0	Note 3
D13	Robustness of terminations	68-2-21 *2036.3 A*	Tension, 40 N, 10 s	4	0	

Note 1 Failure criteria for Thyristors: I_{RRM}, I_{DRM} (T_{vj} max) < 1.1 USL
I_{GT}, V_{GT} (25 °C) < 1.1 USL
V_{TM} (T_{vj} max) < 1.1 USL

Note 2 Failure criteria for all Puck decices: Integrity of package materials, wafers, sealing, lead connections. The device must meet requirements listed under note 1.

Note 3 Failure criteria for all Puck devices: No significant corrosion.

4.6 Product Traceability and Failure Analysis

Product traceability from production, through assembly and test to the customer and finally into service, is assured by relating all manufacturing and test data to a unique batch and device number. This number is engraved on the component flange.

Failure Analysis and Customer Complaints

Should anomalies be detected at the customer's receiving inspection, on his production line (test of sub-systems or systems), or in the event of field failures, ABB Semiconductors' Quality and Reliability Department focuses the company's resources on finding the root cause of failure and in implementing corrective actions. Using circumstantial information from the customer, together with state-of-the-art analytical techniques such as electron beam microscopy and EDX analysis, the Failure Analysis Lab establishes a failure mode report which is sent to the customer and circulated internally to initiate corrective actions where required.

4.7 Related Documents and Standards

- IEC Publication 68, Basic environmental testing procedures
- IEC Publication 747-6, Semiconductor devices, Discrete devices and integrated circuits, Part 6: Thyristors
- IEC Publication 749, Semiconductor devices, Mechanical and climatic test methods
- Military Standard MIL-STD-750C, Test methods for semiconductor devices
- 5SYC 0050-01, General Quality Specification for High Power Semiconductors, ABB Semiconductors AG